(12) UK Patent Application (19) GB (11) 2 370 414 (13) A

(43) Date of A Publication 26.06.2002

(21) Application No 0117316.0

(22) Date of Filing 16.07.2001

(30) Priority Data
(31) 09621110 (32) 21.07.2000 (33) US

(51) INT CL[7]
H01L 23/498 // H01L 21/58 23/50

(52) UK CL (Edition T)
H1K KRD K4C11 K4C3E K5D9 K5M2

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(58) Field of Search
UK CL (Edition T) H1K KRD KRE KRF KRJ KRLX KRM KRX
INT CL[7] H01L
ONLINE: WPI, EPODOC, JAPIO

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(54) Abstract Title
Method of manufacturing integrated circuit package with cavity to expose lower conductive level

(57) A method of manufacturing an integrated circuit package involves providing a multi-layered substrate (10) having a conductive layer (30) between two dielectric layers (20, 22), where a cavity is formed in one of the dielectric layers (22). The cavity exposes conductive layer (30) to enable coupling of integrated circuit (IC) chip (75) to the exposed portion of conductive layer (30). The conductive layer (30) may be coupled to bond pads on the IC chip (75) through wires (80). A ground plane or a power plane may be provided in the exposed portion of the conductive layer (30), which may also provide a connection for a signal line. The package may include a further conductive layer (32) above dielectric layer (22). The IC package may be a ball grid array (BGA) integrated circuit package having solder balls (65) connected to IC chip (75) by plated through holes in substrate (10).

FIG. 6

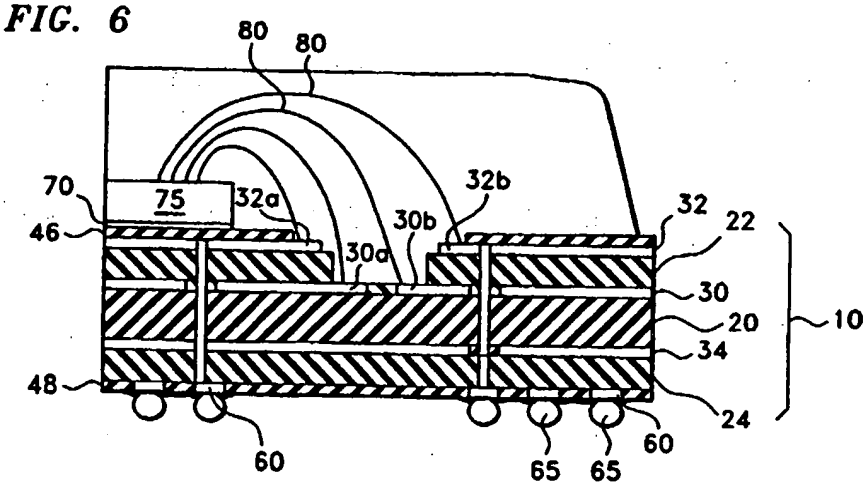

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FIG. 1

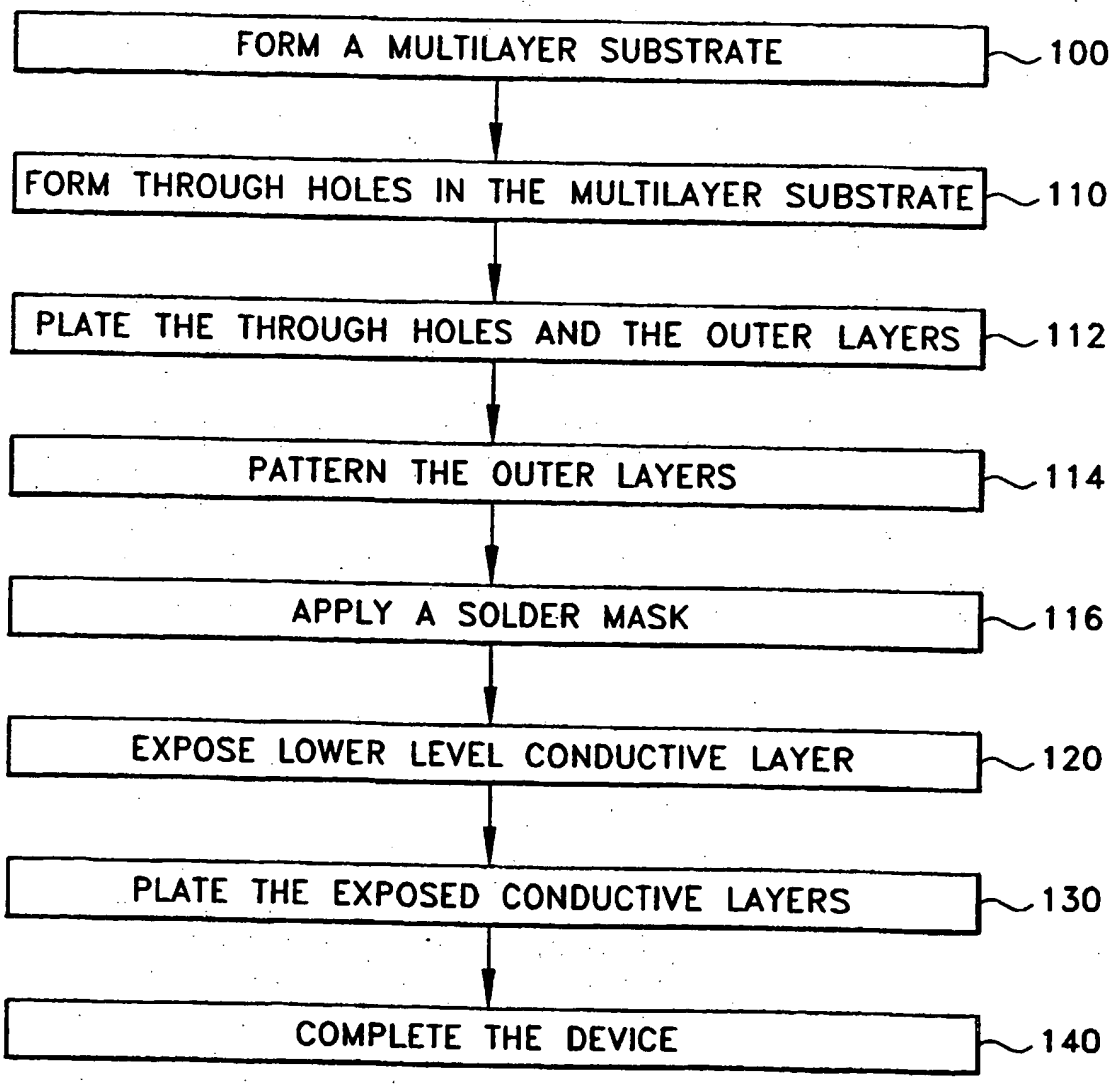


FIG. 2

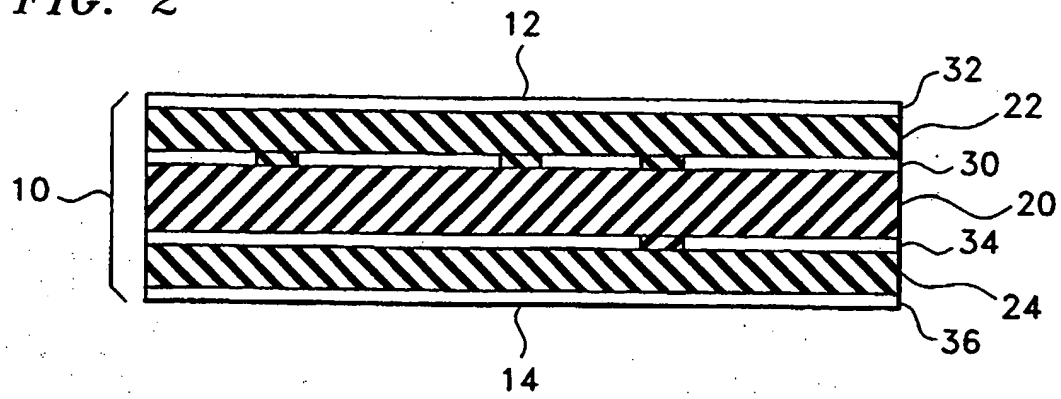


FIG. 3

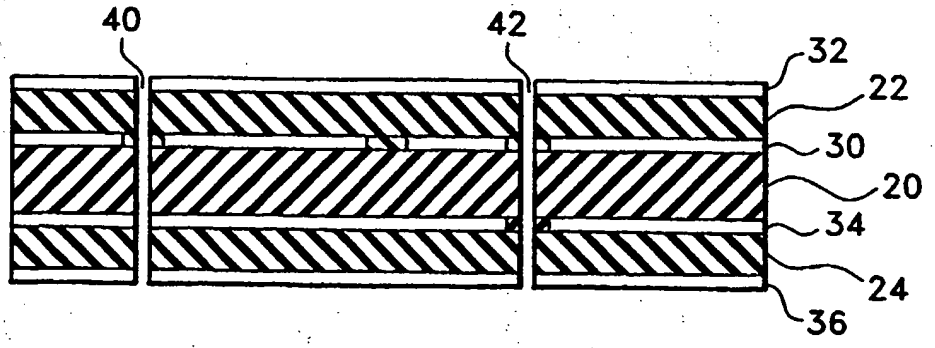
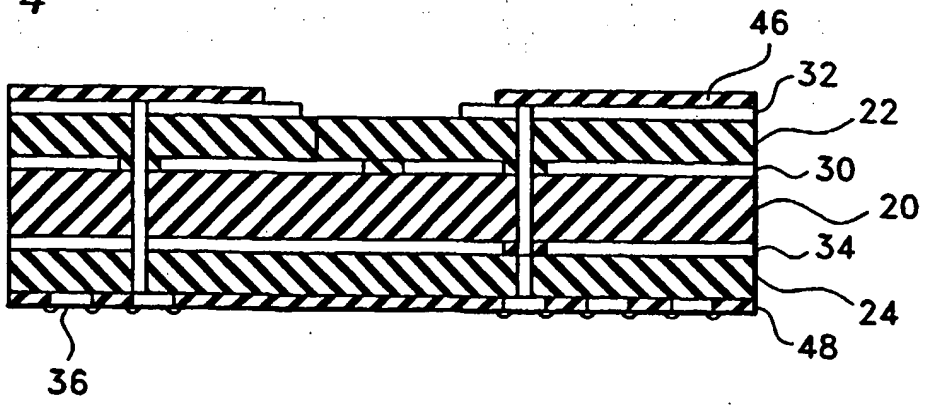


FIG. 4



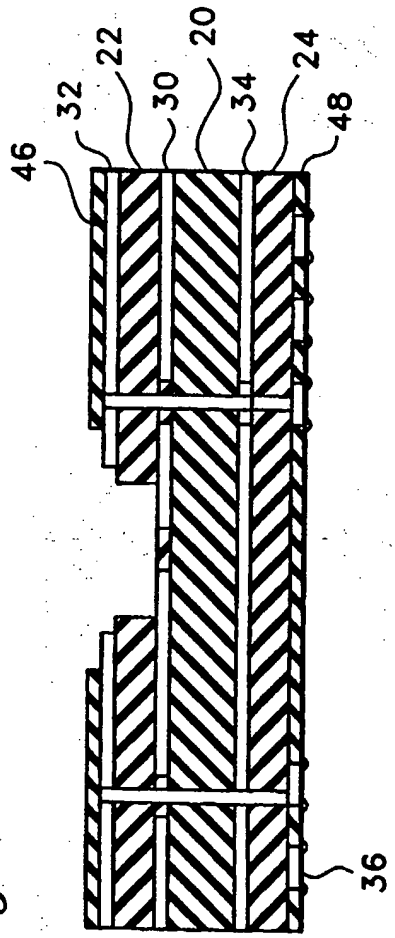


FIG. 5

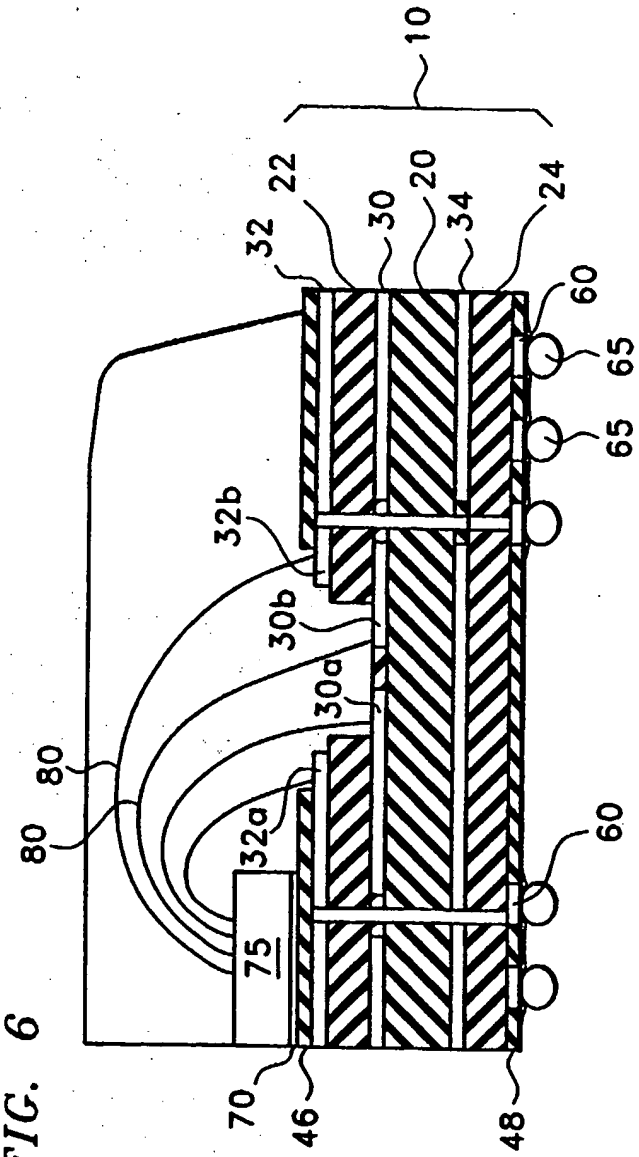
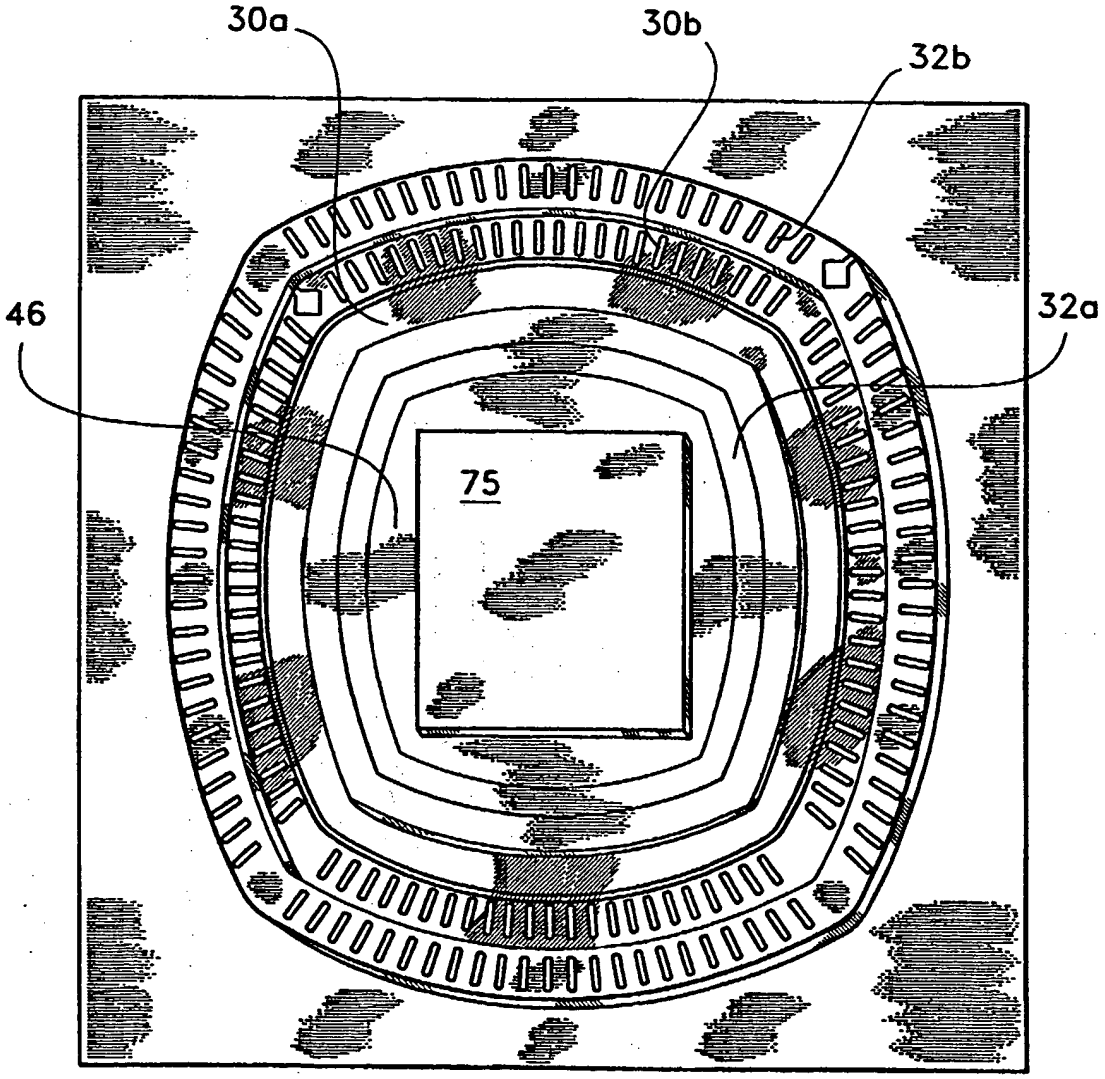


FIG. 6

FIG. 7



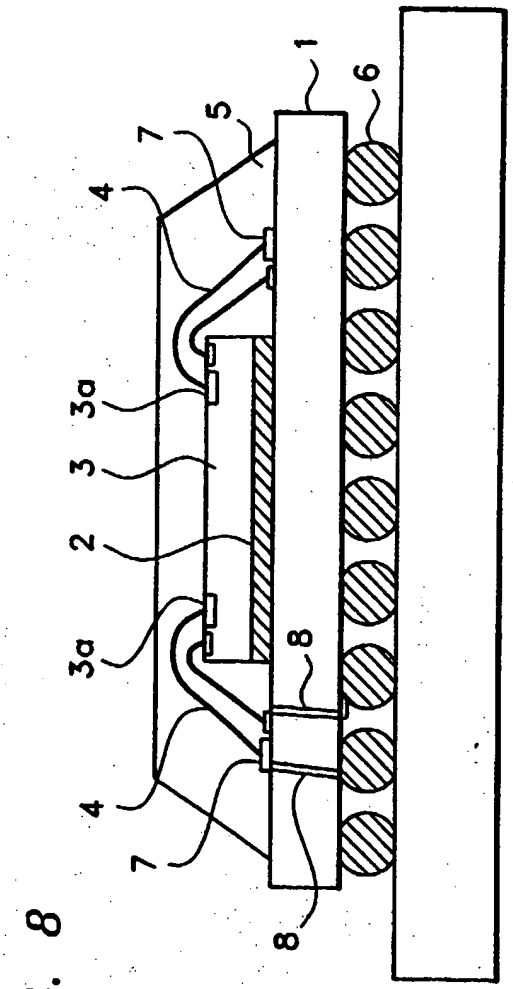


FIG. 8

A METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT PACKAGE

Field of the Invention

The present invention relates generally to integrated circuits and, more particularly, to methods for manufacturing packages for integrated circuits and methods for manufacturing those packages.

Background of the Invention

Ball grid array (BGA) integrated circuit packages (hereinafter BGA packages) are widely used for mounting integrated circuit chips because they provide several advantages over other packaging technologies. BGA packages allow multiple pin structures to be mounted in limited surface areas. Further, BGA packages are less susceptible to impact damage because the outer terminals of the BGA package are short and stubby. In addition, the BGA package has relatively short bond pad to solder ball traces that result in improved electrical performance.

Fig. 8 illustrates a typical BGA package. The BGA package includes a substrate 1, which may consist of a double sided or multilayer structure, an integrated circuit chip 3 mounted on the upper surface of the substrate 1 by an adhesive 2. Metal wires 4 electrically interconnect a plurality of bond pads 3a formed on the upper surface of the integrated circuit with bond pads 7 formed on the substrate 1. Also provided is a molding section 5 formed on the upper surface of the substrate 1 to encapsulate the integrated circuit chip 3 and the metal wires 4. Solder balls 6 are attached on the lower surface of the substrate 1. The bond pads 7 are connected to the solder balls 6 using plated through holes 8 formed in the substrate 1.

To fabricate this BGA package, the integrated circuit chip 3 is attached to the upper central portion of the substrate 1 by an adhesive 2 in a die bonding process. Thereafter, in a wire bonding process, the bond pads 3a formed on the upper surface of the integrated circuit 3 and the bond pads 7 formed on the substrate 1 are interconnected with the metal wires 4. Using a molding process, the integrated circuit 3, the metal wires 4, and a portion of the upper surface of the substrate 1 are encapsulated with epoxy to form the molding section 5. In a solder ball attaching process, the solder balls 6 are attached to the lower surface of the substrate 1.

While this BGA package provides advantages it does, however, have its drawbacks. For example, a large number of through holes are formed in the

substrate 1, of a multilayer metallization structure, between the power and ground rings, and the respective internal planes. As a result, the electrical performance is degraded because the conductive paths for current flow through the internal power and ground planes are reduced. Accordingly, it is desirable to develop a BGA package that reduces this problem.

Summary of the Invention

The present invention is directed to a process for manufacturing an integrated circuit package such as a BGA package for use with an integrated circuit chip. The substrate of the integrated circuit package is formed having a cavity that exposes a lower conductive level in the substrate so that connections between the integrated circuit and the lower conductive level may be formed; thus reducing the need for plated through hole connections from conductive layer to conductive layer. As a result, the conductive paths in the internal power and ground planes are not necessarily cut off by the plated through holes thus avoiding or reducing some of the electrical performance degradation suffered by prior techniques. In addition, the invention allows more signals to be added and/or the size of the integrated circuit to be reduced for enhanced electrical performance. The multiple bonding tier integrated circuit package may also provide greater wire separation that eases wire bonding and subsequent encapsulation processes.

Illustratively, the substrate of the integrated circuit package includes a conductive layer formed above a first dielectric layer and a second dielectric layer formed above the first conductive layer. The second dielectric layer has a cavity exposing a portion of the first conductive layer. Also provided is an integrated circuit, positioned above the second dielectric layer, coupled to the exposed portion of the first conductive layer.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

Brief Description of the Drawing

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice in the semiconductor industry, the various features of the drawing are not to scale. On the contrary, the dimensions of

the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a flow chart diagram illustrating an exemplary process of the present invention for manufacturing a ball grid array package;

Figs. 2-6 are schematic diagrams of a ball grid array substrate during successive stages of manufacture according to the process shown in Fig. 1;

Fig. 7 is a top view of the ball grid array substrate shown in Fig. 5; and

Fig. 8 is a schematic diagram of a conventional ball grid array package.

Detailed Description of the Invention

Referring now to the drawing, wherein like reference numerals refer to like elements throughout, Fig. 1 is a flow chart diagram illustrating the process for manufacturing an integrated circuit package according to an exemplary embodiment of the present invention. The process shown in Fig. 1 is described below with reference to Figs. 2-6.

At step 100, a multilayer substrate 10 (Fig. 2) is provided. The process for manufacturing the multilayer substrate 10 is well known. The substrate includes insulating layers 20, 22, 24 and conductive layers 30, 32, 34, 36. The conductive layers 30, 32, 34, 36 may be patterned using standard techniques. These layers are patterned to form interconnections from the top 12 to the bottom 14 of the multilayer substrate 10. Conductive layers 30, 32, 34, 36 may be a metal such as copper or other suitable conductive material.

At step 110, through holes such as 40 and 42 (Fig. 3) are formed in the multilayer substrate 10 using standard processes. For example, the through holes may be formed by mechanical or laser drilling of the multilayer substrate 10. Although two through holes 40 and 42 are shown, a number of through holes may be formed in the multilayer substrate 10.

Next, at step 112, the through holes 40 and 42 and the outer conductive layers are plated. The outer conductive layers include conductive layers 32 and 36. The plating process includes forming a seed layer on the exposed surfaces including the through holes followed by an electroless plating flash and electroplating. The plating materials includes, for example, copper. At step 114, the conductive layers 32 and 36 are patterned using well-known processes. Then, at step 116, a solder mask 46

and 48 is applied to the conductive layers 32 and 36 and patterned to expose portions of the conductive layers 32 and 36 and insulating layer 22.

Next, at step 120, a cavity 50 (Fig. 5) is formed in the insulating layer 22 to expose conductive layer 30. Cavity 50 may be formed by routing, laser milling, plasma etching, or other cavity forming techniques. By exposing the conductive layer 30, wire bonds from the integrated circuit may be formed directly to at least two different bonding tiers within the multilayer substrate 10.

One or more of the exposed portions of the conductive layer 30 may form a power plane, ring or area. In this case, multiple bond pads of the integrated circuit may be interconnected to the exposed plane, ring, or area. Instead of a power plane, the exposed portions of the conductive layer 30 may form a ground plane. In this way, the need for multiple through holes for connecting to power or ground may be reduced or eliminated. Portions of the exposed conductive layer 30 may also include a combination of areas including one or more of a ground plane, power plane, or connections for signal lines.

At step 130, a conductive wire bondable material is formed on the exposed conductive areas of conductive layers 30, 32 and 36. The conductive material may include gold formed on nickel. In this case, nickel is plated onto the exposed portions of conductive layers 30, 32, and 36 and gold is plated onto the nickel.

At step 140, the device is completed (Fig. 6). This includes coupling an integrated circuit chip 75 to the multilayer substrate 10 using an adhesive 70. Wire bonds 80 are formed between bond pads (not shown) on the integrated circuit and connection areas and/or bond pads 30a, 30b, 32a, 32b on the multilayer substrate 10. The connection areas are areas such as bond pads where the wires may be directly connected to conductive layers 30 and 32. In addition, the integrated circuit chip and the wire bonds are overmolded with an epoxy and solder balls 65 are coupled to the connecting pads 60 (formed from conductive layer 36) using conventional techniques.

In the illustrative embodiment, the integrated circuit chip 75 is formed on a segment of the mask 70 (Figs. 6 and 7). While only one wire bond is shown coupled to the ground plane, a plurality of wire bonds may be used to interconnect the integrated circuit 75 and the ground plane 32a. As a result, a plurality of through holes do not have to be formed in the multilayer substrate 10 for interconnecting the integrated circuit 75 to ground.

In addition, segment 30a of the conductive layer 30 may form a power plane and be electrically coupled to the integrated circuit chip 75. While only one wire bond is shown coupled to the power ring 30a, a plurality of wire bonds may be used to interconnect the integrated circuit chip 75 and the power plane 30a. As a result, a plurality of through holes do not have to be formed in the multilayer substrate 10 for interconnecting the integrated circuit chip 75 to the power plane 30a. Alternatively, segment 30b may form the power plane. The power plane, the ground plane, or other segment of the conductive layers may be formed as a continuous region along one, two, three or more sides of the integrated circuit or they may encircle the integrated circuit.

Although the invention has been described with reference to exemplary embodiments, it is not limited to those embodiments. For example, the exemplary embodiments described above include four conductive layers, however, the invention is applicable to substrates that include three or more conductive layers and associated insulating layers for separating those conductive layers. In addition, cavities may be formed in more than one of the dielectric layers of the substrate exposing one or more of the conductive layers in the substrate. Further, connections for signal lines, power, or ground, or combinations thereof, may be provided in the cavity of the substrate. Accordingly, the appended claims should be construed to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the true spirit and scope of the present invention.

What is Claimed:

1. A process for manufacturing an integrated circuit package comprising:

(a) providing a substrate having a first dielectric layer, a conductive layer above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity exposing a portion of the conductive layer; and

(b) interconnecting an integrated circuit directly to the exposed portion of the conductive layer in the cavity.

2. The method of claim 1 wherein step (b) comprises:

coupling a conductor to a bond pad formed on the integrated circuit; and

connecting the conductor directly to the conductive layer.

3. The method of claim 1 further comprising providing one of a ground plane and a power plane in the exposed portion of the conductive layer.

4. The method of claim 3 further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer.

5. The method of claim 1 further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer.

6. The method of claim 1 further comprising forming multiple interconnections between the integrated circuit chip and the conductive layer.

7. A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) providing a first dielectric layer;

(b) providing a conductive layer above the first dielectric layer;

(c) providing a second dielectric layer above the conductive layer; and

(d) forming a cavity in the second dielectric layer to expose a portion of the conductive layer.

8. The method of claim 7 wherein steps (a), (b), and (c) occur prior to step (d).

9. The method of claim 7 further comprising:

providing a contact area to a ground plane by exposing the portion of the conductive layer.

10. The method of claim 7 further comprising:

(e) forming plated through holes in the substrate.

11. The method of claim 10 wherein step (e) is performed prior to step (d).

12. A method of manufacturing an integrated circuit package comprising:

providing the substrate of claim 7; and

coupling the integrated circuit chip to the substrate.

13. A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) providing a first dielectric layer;

(b) providing a first conductive layer above the dielectric layer;

(c) providing a second dielectric layer above the first conductive layer;

(d) providing a second conductive layer above the second dielectric layer;

(e) forming a cavity in a first region of the second dielectric layer to expose a portion of the first conductive layer.

14. The process of claim 13 wherein step (d) further comprises providing the second conductive layer on regions other than the first region.

15. The process of claim 13 wherein step (d) further comprises removing a portion of the conductive layer formed above the first region.

16. A method of manufacturing an integrated circuit package comprising:

providing the substrate of claim 13; and

coupling the integrated circuit chip to the substrate.

17. A process for manufacturing an integrated circuit package comprising:

(a) receiving a substrate having a first dielectric layer, a conductive layer above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity exposing a portion of the conductive layer; and

(b) interconnecting an integrated circuit directly to the exposed portion of the conductive layer in the cavity.

Application No: GB 0117316.0 **Examiner:** T P Marlow
Claims searched: 1 to 17 **Date of search:** 15 April 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H1K: (KRD) (KRE) (KRF) (KRJ) (KRLX) (KRM) (KRX)

Int Cl (Ed.7): H01L

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2077036 A	CTS - see dielectric layer (14,18) and conductive layer (46) connected to IC chip (40) in Fig. 3	1-9,12-17
X	EP 1011139 A1	IBIDEN - see electronic component (61), conductive layer (12) between dielectric layer (21,22), cavity (5) and through holes (2) in Figs. 8 to 10	1-17
X	EP 0849793 A2	TEXAS INSTRUMENTS - see conducting layers (251,252) connected to ground pins, and conducting layers (221,222) connected to signal pins with cavity in Fig. 5	1-9,12-17
X	EP 0678918 A2	HITACHI - see dielectric layers and conducting layers exposed by cavity, and plated through holes in Fig. 10	1-17
X	EP 0645811 A2	TOSHIBA - see dielectric layer (21,22) and conductive layers (24) connected to integrated circuit (11) in Fig. 1A	1-9,12-17

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Application No: GB 0117316.0 **Examiner:** T P Marlow
Claims searched: 1 to 17 **Date of search:** 15 April 2002

Category	Identity of document and relevant passage		Relevant to claims
X	WO 96/23612 A1	HESTIA - see core layer (58) with surface conducting layer connected to IC chip (50) exposed by cavity (44) and through hole (56) in Fig. 11	1-17
X	US 5689091	VLSI TECHNOLOGY - see Figs. showing conducting layer (12a) between non-conductive layers (10,24a) with conducting layer exposed by forming cavity and connected to IC chip (38)	1-17
X	US 5490324	LSI LOGIC - see Fig. 4 showing conductive layer (438) between dielectric layers (402,404) where layer (438) is exposed by forming cavity housing chip (406)	1-9,12-17

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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